6.2 A CMOS Carrier-less UWB Transceiver for WPAN Applications

Yuanjin Zheng[1], Yan Tong[1,2], Chyuen Wei Ang[1,2], Yong-Ping Xu[2], Wooi Gan Yeoh[1], Fujiang Lin[1], Rajinder Singh[1]

[1]Institute of Microelectronics, Singapore
[2]National University of Singapore, Singapore

UWB communication has great potential for low-cost high-quality broadband multimedia applications, especially for wireless personal area networking applications [1]. Typically, an UWB transceiver can employ either the direct-sequence UWB (DS-UWB) or MB-OFDM scheme, but both techniques need LOs for RF up/down-conversion and require complex systems. In this work, a carrier-less impulse-radio-based high-rate UWB transceiver utilizing a new modulation scheme is developed, which uses fewer components and consumes less power. The CMOS transceiver works in the FCC–approved low band from 3.1 to 5GHz.

Figure 6.2.1 shows the block diagram of the impulse-based UWB transceiver. The TX generates pulse-position modulated (PPM) UWB high-order derivative pulses that are then emitted by the UWB antenna. At the RX, the received pulses are weak and are first amplified by the LNA. The amplified pulses are then correlated with the local pulses, further amplified and integrated to a constant level for A/D conversion. As such, the signal modulation and demodulation are both completed in the analog domain.

The transmitter circuits and simplified modulation scheme are shown in Fig. 6.2.2. A CMOS pulse generator (PG) circuit is employed to generate Gaussian monocycle pulses, which are the second derivative of Gaussian pulses [2]. Positive and negative UWB monocycle pulses occupying the frequency band from 900MHz to 5GHz are generated on the rising and falling edges of an input digital pulse respectively. In order to meet the FCC spectral mask, these pulses are further amplified and shaped. After being amplified by a wideband pulse amplifier (WPA), the pulses are then shaped by a pulse shaping amplifier (PSA). The PSA utilizes a common source-common gate (CS-CG) cascode configuration (M6 and M7) with wideband LC input matching (C3, C4, and L3 to L6). The output of the PSA is matched to the TX antenna. Together, the input and output LC networks of the PSA act as a third-order derivative circuit. As a result, the TX output pulses are shaped into the fifth derivative of Gaussian pulses that meet the 3.1 to 5GHz FCC mask. The combined power gain of the WPA and the PSA is 14.5dB, and the output power is -9dBm.

As shown in Fig. 6.2.2, a PPM scheme is proposed to directly modulate the digital baseband signals to UWB pulses. The baseband NRZ (non-return-to-zero) data (a) are used to drive the TX PG. Since each pair of input data edges generate a pair of UWB fifth-derivative-of-Gaussian pulses through the TX circuits, the locations of the generated pulses (b) are therefore modulated by the digital data (a). At the RX, the first derivative of the Gaussian pulses (c) are generated and synchronized to the received pulses (b), and the multiplication of (b) and (c) generates (d). The integrated outputs (e) (to the integral of (d)) recover the transmitted data (a). A measured pulse sequence at the TX output and its spectrum are shown in Fig. 6.2.3. The generated pulses are approximately the fifth derivative of Gaussian pulses with 1.5ns width and maximum swing of $195mV_{pp}$. The spectrum of the pulse sequence fits into the FCC mask.

A three-stage wideband LNA is implemented as shown in Fig. 6.2.4. The first stage employs a CS-CG cascode structure (M1 and M2) with wideband LC ladder matching (L1/L2 and C1/C2), which boosts the gain, minimizes the noise figure (NF) and is easily matched to the RX antenna [3]. While in the last two stages, each stage is essentially an inductively peaked shunt feedback amplifier. The feedback loop formed by C4, M3 and L5 is used for BW expansion. Since only one transistor is used at the output stage, linearity can be ensured. The LNA achieves a measured power gain of 20.2dB, NF of 4.6dB, and -3dB BW of 4.5GHz. The correlation of received pulses with local pulses needs a highly linear and wideband multiplier. The multiplier used is shown in Fig. 6.2.4 and attains a ±85mV linear region for the RF input. To improve the correlation gain, the LO input comes from a differential PG, which generates the first-derivative-of-Gaussian pulses with amplitudes of $210mV_{pp}$ and 0.7ns width [2]. Inductive peaking is employed to extend the BW of the multiplier. The multiplier has a measured 4.6dB conversion gain and 7.5GHz BW.

The LPF follows to reject strong out-of-band interference and suppress the high-frequency pulse signals that leak through the multiplier. A third-order elliptical LC ladder filter is implemented with a cut-off frequency of 250MHz. The filter also acts as the load for a differential amplifier [4]. The gain of the two-stage cascaded variable gain amplifier can vary from -10 to 45dB with a 300MHz bandwidth. A low-pass feedback loop is employed to reject the dc offset with cutoff frequency 600kHz. The Gm-C-OTA integrator achieves a low -3dB bandwidth of 1MHz and a high unit-gain bandwidth of 1GHz. This provides a high integration gain and a long holding time. The steady integration value can hold for 10ns with only <1% error due to charge leakage.

A separate ADC chip employing a flash architecture and 4b resolution is adopted for further signal processing in baseband. A PLL with a ring oscillator is used for clock generation while two cascaded delay-locked loops (DLL) are used for synchronization. The two DLLs are capable of delaying the clock with minimum steps of 1ns and 0.1ns respectively. During pulse acquisition, the baseband synchronizer detects the amplitude of the correlated output and then delays the clock using the DLL until the correlated output is larger than a pre-determined threshold. Subsequently, an early-late tracking loop is employed to lock the local pulses with the received pulses. Once the synchronization (acquisition and tracking) is sustained, coherent demodulation will take place.

The transceiver IC is integrated in a 0.18μm CMOS technology utilizing a die area of $2.6\times1.7mm^2$. Typical measured transmit data patterns (at TX input), emitted pulse patterns (at TX output), and demodulated data patterns (at RX integrator output) for data rates of 100Mbps and 200Mbps are shown in Fig. 6.2.5. The measured RX performance includes a NF of 7.7 to 8.1dB, IIP3 of -12.3dBm, sensitivity of -80 to -72dBm, while the measured power consumption is 76mW for the TX and 81mW for the RX, both from a 1.8V supply. The transceiver performance is summarized in Fig. 6.2.6. The chip micrograph is shown in Fig. 6.2.7.

Acknowledgement:
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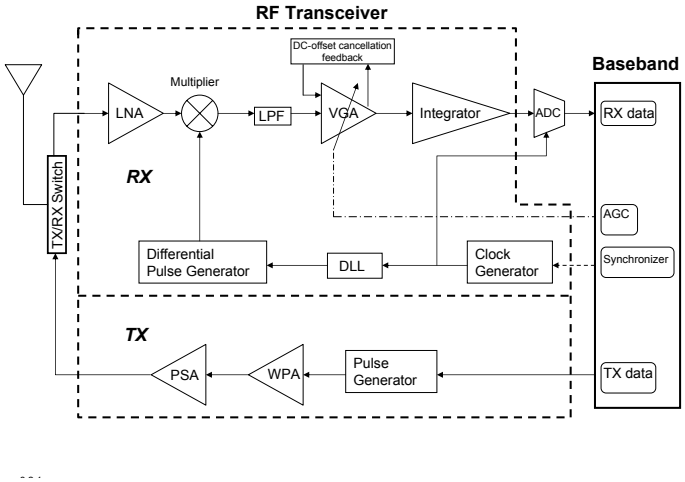

Figure 6.2.1: UWB transceiver system diagram.

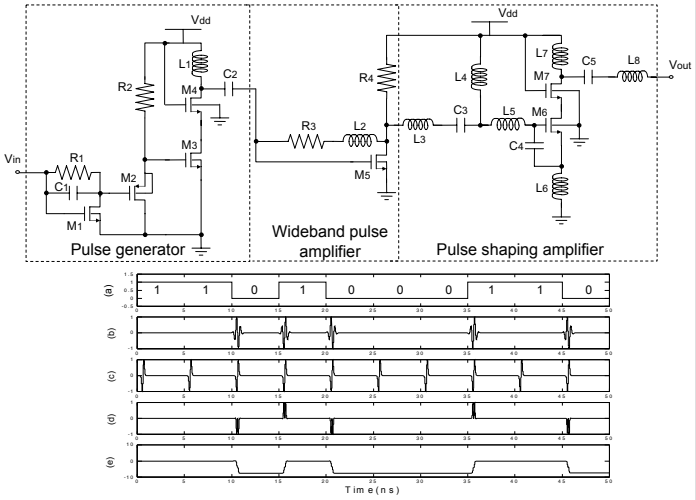

Figure 6.2.2: Pulsed TX circuits and modulation/demodulation scheme.

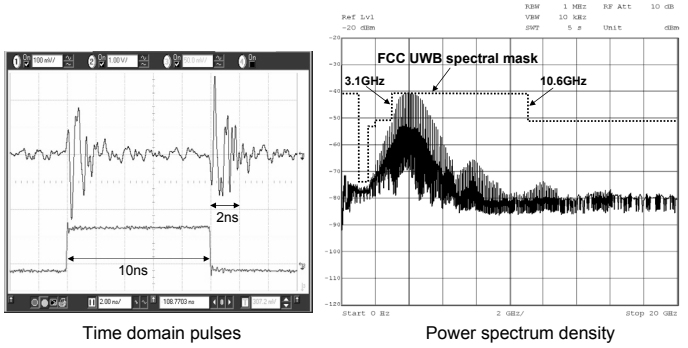

Figure 6.2.3: Measured UWB pulses and spectrum.

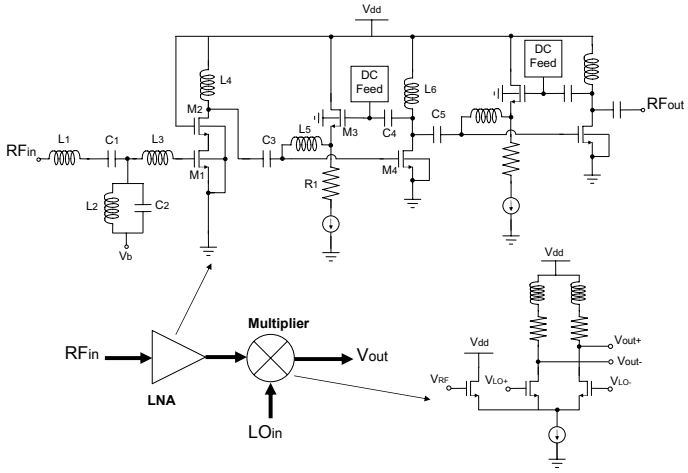

Figure 6.2.4: LNA and multiplier.

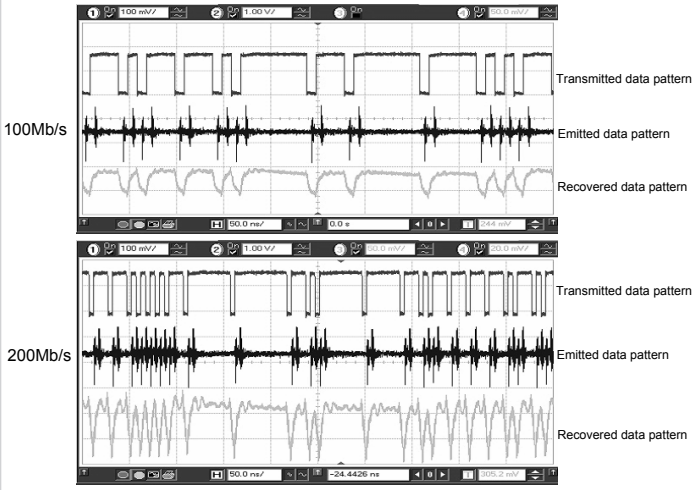

Figure 6.2.5: Measured TRX outputs (data rate 100Mb/s and 200Mb/s).

Receiver		Transmitter	
RX Noise Figure	7.7 to 8.1dB	Transmitted Power	-9dBm
RX Gain (maximum)	83.5dB	Pulse Width	<1ns
IIP3 at Max Gain	-12.3dBm @ 4.1GHz	Pulse Bandwidth (-10dB)	2GHz
IIP3 at Reduced Gain	-2.1dBm @ 4.1GHz	TX Power Dissipation	76mW
RX P-1 dB	-22dBm @ 4.1GHz	TX Rate (maximum)	400Mbps
Sensitivity	-80 to -72dBm		
VGA Gain Range	-10 to 45dB	Modulation	PPM/coherent
RX Power Dissipation	81mW		
ADC		**Overall**	
ADC Resolution	4bits	Supply Voltage	1.8V
ADC Sampling Rate (maximum)	500MSamples/s	Technology	CMOS 0.18-µm
ADC Power	80mW	TRX Die Size	2.6mm × 1.7mm

Figure 6.2.6: Summary of transceiver performance.

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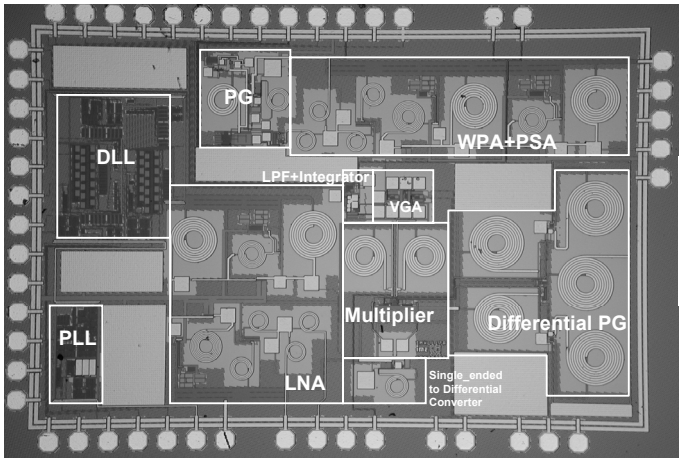

Figure 6.2.7: TRX chip micrograph.

